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<u>L8</u>	(input near3 (buffer or register)) near8 (input signal)	6259	<u>L8</u>
<u>L7</u>	(11 near6 (activat\$3 or enabl\$4)) with ((chang\$4 or differ\$3 or var\$4 or match\$4 or compar\$4 or correspond\$4) near4 (input near4 (signal or buffer)))	15	<u>L7</u>
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<u>L3</u>	input near4 buffer	57310	<u>L3</u>
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### 1 [Fast detection of communication patterns in distributed executions](#)

Thomas Kunz, Michiel F. H. Seuren

November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on**

Full text available: [pdf\(4.21 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [refere](#)

Understanding distributed applications is a tedious and difficult task. Visualizations based on proce the execution of the application. The visualization tool we use is Poet, an event tracer developed a very complex and do not provide the user with the desired overview of the application. In our expi commun ...

### 2 [Interactive Editing Systems: Part II](#)

Norman Meyrowitz, Andries van Dam

September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3

Full text available: [pdf\(9.17 MB\)](#)

Additional Information: [full citation](#), [references](#), [citings](#), [ind](#)

### 3 [On embedding a microarchitectural design language within Haskell](#)

John Launchbury, Jeffrey R. Lewis, Byron Cook

September 1999 **ACM SIGPLAN Notices , Proceedings of the fourth ACM SIGPLAN internati**

Full text available: [pdf\(1.26 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [refere](#)

Based on our experience with modelling and verifying microarchitectural designs within Haskell, th language. In particular, we highlight our use of Haskell's lazy lists, type classes, lazy state monad, could be improved in the future. We end with an example of a benefit gained by bringing the funct

### 4 [An Unclever Time-Sharing System](#)

Caxton C. Foster

January 1971 **ACM Computing Surveys (CSUR)**, Volume 3 Issue 1

Full text available: [pdf\(1.85 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [refere](#)


This paper describes the internal structure of a time-sharing system in some detail. This system is structure. It is intended for use in a university type environment where there are many short jobs simplicity, this system can serve as a useful introduction to the problems encountered by the desi comman ...

##### 5 Operational characteristics of a hardware-based pattern matcher

Roger L. Haskin, Lee A. Hollaar

March 1983

**ACM Transactions on Database Systems (TODS)**, Volume 8 Issue 1

Full text available:  pdf(1.84 MB)

Additional Information: [full citation](#), [abstract](#), [refere](#)

The design and operation of a new class of hardware-based pattern matchers, such as would be used in a retrieval system, is presented. This recognizer is based on a unique implementation technique for among a number of simple digital machines. It avoids the problems generally associated with implementing complex control ...

**Keywords:** backend processors, computer system architecture, finite state automata, full text retrieval

##### 6 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000

**ACM Transactions on Design Automation of Electronic Systems (TODAES)**,

Full text available:  pdf(385.22 KB)

Additional Information: [full citation](#), [abstract](#), [refere](#)

This tutorial surveys design methods for energy-efficient system-level design. We consider electro We consider the three major constituents of hardware that consume energy, namely computation, reducing their energy consumption. We also study models for analyzing the energy cost of software compilation. This survey ...

##### 7 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996

**ACM Transactions on Design Automation of Electronic Systems (TODAES)**,

Full text available:  pdf(550.02 KB)

Additional Information: [full citation](#), [abstract](#), [refere](#)

Low power has emerged as a principal theme in today's electronics industry. The need for low power as important as performance and area. This article presents an in-depth survey of CAD methodology and systems and describes the many issues facing designers at architectural, logical, and physical tool ...


**Keywords:** CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, low power synthesis, lower-power design, power analysis and estimation, power management, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic

##### 8 Human-computer interface development: concepts and systems for its management

H. Rex Hartson, Deborah Hix

March 1989

**ACM Computing Surveys (CSUR)**, Volume 21 Issue 1

Full text available:  pdf(7.97 MB)

Additional Information: [full citation](#), [abstract](#), [refere](#)

*Human-computer interface management*, from a computer science viewpoint, focuses on the process of representation, design, implementation, execution, evaluation, and maintenance. This survey presents independence, structural modeling, representation, interactive tools, rapid prototyping, development methods ...

##### 9 Abstract state machines capture parallel algorithms

Andreas Blass, Yuri Gurevich

October 2003

**ACM Transactions on Computational Logic (TOCL)**, Volume 4 Issue 4

Full text available:  pdf(610.28 KB)

Additional Information: [full citation](#), [abstract](#), [refere](#)

We give an axiomatic description of parallel, synchronous algorithms. Our main result is that every state machine with a background that provides for multisets.


**Keywords:** ASM thesis, Parallel algorithm, abstract state machine, postulates for parallel comput

**10** Micropipelines

I. E. Sutherland

June 1989

**Communications of the ACM**, Volume 32 Issue 6

Full text available:  pdf(2.30 MB)

Additional Information: [full citation](#), [abstract](#), [refere](#)

The pipeline processor is a common paradigm for very high speed computing machinery. Pipeline | operate concurrently, much as different people on a manufacturing assembly line work concurrent pipeline processors makes their design a demanding task, they can be found in graphics processor doing arit ...

**11** Pipeline Architecture

C. V. Ramamoorthy, H. F. Li

January 1977 **ACM Computing Surveys (CSUR)**, Volume 9 Issue 1

Full text available:  pdf(3.53 MB)


Additional Information: [full citation](#), [references](#), [citing](#), [index terms](#)

**12** System architectures for computer music

John W. Gordon

June 1985

**ACM Computing Surveys (CSUR)**, Volume 17 Issue 2

Full text available:  pdf(4.61 MB)

Additional Information: [full citation](#), [abstract](#), [refere](#)


Computer music is a relatively new field. While a large proportion of the public is aware of comput better understanding of its capabilities and limitations in terms of synthesis, performance, and rec discussing the architecture of existing computer music systems. System requirements vary accord

**13** The family of concurrent logic programming languages

Ehud Shapiro

September 1989

**ACM Computing Surveys (CSUR)**, Volume 21 Issue 3

Full text available:  pdf(9.62 MB)

Additional Information: [full citation](#), [abstract](#), [refere](#)


Concurrent logic languages are high-level programming languages for parallel and distributed syst programming techniques. Being logic programming languages, they preserve many advantages of of programs and computations, the convenience of representing data structures with logical terms metaprogrammin ...

**14** Pen computing: a technology overview and a vision

André Meyer

July 1995

**ACM SIGCHI Bulletin**, Volume 27 Issue 3

Full text available:  pdf(5.14 MB)

Additional Information: [full citation](#), [abstract](#), [citing](#)

This work gives an overview of a new technology that is attracting growing interest in public as we other technologies is in the use of a pen or pencil as the primary means of interaction between a u metaphor. From this follows a set of consequences that will be analyzed and put into context with historic ...

**15** Flexible collaboration transparency: supporting worker independence in replicated applicatio

James Begole, Mary Beth Rosson, Clifford A. Shaffer

June 1999

**ACM Transactions on Computer-Human Interaction (TOCHI)**, Volume 6 Issue 2

Full text available:  pdf(312.22 KB)

Additional Information: [full citation](#), [abstract](#), [refere](#)



This article presents a critique of conventional collaboration transparency systems, also called "ap

of legacy single-user applications. We find that conventional collaboration transparency systems a key groupware principles: concurrent work, relaxed WYSIWIS, and group awareness. Next, we pre

**Keywords:** Flexible JAMM, Java, application sharing, collaboration transparency, computer-suppo

# 16 Razor: A Low-Power Pipeline Based on Circuit-Level Timing Speculation

Dan Ernst, Nam Sung Kim, Shidhartha Das, Sanjay Pant, Rajeev Rao, Toan Pham, Conrad Ziesler, D  
December 2003 **Proceedings of the 36th Annual IEEE/ACM International Symposium on M**

Full text available:  [pdf\(568.17 KB\)](#)  [Publisher Site](#)

Additional Information: [full citation](#), [abstract](#)

With increasing clock frequencies and silicon integration, power aware computing has become a cri  
chip. One of the more effective and widely used methods for power-aware computing is dynamic vo  
from DVS, it is essential to scale the supply voltage as low as possible while ensuring correct operat  
worst-case ...

# 17 Curriculum 68: Recommendations for academic programs in computer science: a report of tl

William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William  
Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young  
March 1968 **Communications of the ACM**, Volume 11 Issue 3

Full text available:  [pdf\(6.63 MB\)](#)

Additional Information: [full citation](#), [references](#), [citi](#)

**Keywords:** computer science academic programs, computer science bibliographies, computer sci  
education, computer science graduate programs, computer science undergraduate programs

# 18 Complexity-effective superscalar processors

Subbarao Palacharla, Norman P. Jouppi, J. E. Smith  
May 1997

**ACM SIGARCH Computer Architecture News , Proceedings of the 24th ann**  
Volume 25 Issue 2

Full text available:  [pdf\(2.21 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [refere](#)

The performance tradeoff between hardware complexity and clock speed is studied. First, a generi  
renaming, instruction window wakeup and selection logic, and operand bypassing are analyzed. Ea  
0.8&micro;m, 0.35&micro;m, and 0.18&micro;m. Performance results and trends are expressed in  
window wakeu ...

# 19 Formal verification in hardware design: a survey

Christoph Kern, Mark R. Greenstreet  
April 1999

**ACM Transactions on Design Automation of Electronic Systems (TODAES),**

Full text available:  [pdf\(411.53 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refere](#)

In recent years, formal methods have emerged as an alternative approach to ensuring the quality  
limitations of traditional validation techniques such as simulation and testing. There are two main  
the formal framework used to specify desired properties of a design and the verification technique

**Keywords:** case studies, formal methods, formal verification, hardware verification, language cor

# 20 Architectures: The SFRA: a corner-turn FPGA architecture

Nicholas Weaver, John Hauser, John Wawrzynek  
February 2004

**Proceeding of the 2004 ACM/SIGDA 12th international symposium on Fiel**

Full text available:  [pdf\(234.25 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [refere](#)

FPGAs normally operate at whatever clock rate is appropriate for the loaded configuration. When f however, it is better to employ fixed-frequency FPGAs operating at a high clock frequency. Such fi which are difficult to support in a traditional FPGA architecture. We have developed a novel approa of logically de ...

**Keywords:** FPGA CAD, FPGA architecture, FPGA design study, FPGA optimization

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